

**WEST**[Generate Collection](#)[Print](#)**Search Results - Record(s) 1 through 20 of 34 returned.**☐ 1. Document ID: US 20030093648 A1

L9: Entry 1 of 34

File: PGPB

May 15, 2003

PGPUB-DOCUMENT-NUMBER: 20030093648

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20030093648 A1

TITLE: Method and apparatus for interfacing a processor to a coprocessor

PUBLICATION-DATE: May 15, 2003

## INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Moyer, William C.	Dripping Springs	TX	US	

US-CL-CURRENT: 712/34

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC
Draw Desc	Image										

☐ 2. Document ID: US 20030028751 A1

L9: Entry 2 of 34

File: PGPB

Feb 6, 2003

PGPUB-DOCUMENT-NUMBER: 20030028751

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20030028751 A1

TITLE: Modular accelerator framework

PUBLICATION-DATE: February 6, 2003

## INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
McDonald, Robert G.	Austin	TX	US	
Williamson, Barry D.	Cedar Park	TX	US	
McDaniel, Micah R.	Austin	TX	US	

US-CL-CURRENT: 712/34

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw Desc	Image									

☐ 3. Document ID: US 20030014611 A1

L9: Entry 3 of 34

File: PGPB

Jan 16, 2003

PGPUB-DOCUMENT-NUMBER: 20030014611  
PGPUB-FILING-TYPE: new  
DOCUMENT-IDENTIFIER: US 20030014611 A1

TITLE: Software for designing, modelling or performing digital signal processing

PUBLICATION-DATE: January 16, 2003

## INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Ferris, Gavin Robert	London		GB	

US-CL-CURRENT: 712/35

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KMC
Draw Desc	Image									

☐ 4. Document ID: US 20030005261 A1

L9: Entry 4 of 34

File: PGPB

Jan 2, 2003

PGPUB-DOCUMENT-NUMBER: 20030005261  
PGPUB-FILING-TYPE: new  
DOCUMENT-IDENTIFIER: US 20030005261 A1

TITLE: Method and apparatus for attaching accelerator hardware containing internal state to a processing core

PUBLICATION-DATE: January 2, 2003

## INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Sheaffer, Gad	Haifa		IL	

US-CL-CURRENT: 712/35

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KMC
Draw Desc	Image									

☐ 5. Document ID: US 20020087829 A1

L9: Entry 5 of 34

File: PGPB

Jul 4, 2002

PGPUB-DOCUMENT-NUMBER: 20020087829  
PGPUB-FILING-TYPE: new  
DOCUMENT-IDENTIFIER: US 20020087829 A1

TITLE: Re-targetable communication system

PUBLICATION-DATE: July 4, 2002

## INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Snyder, Walter L.	San Jose	CA	US	
Tsui, Ernest T.	Cupertino	CA	US	

US-CL-CURRENT: 712/34

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KMC
Draw Desc	Image									

☐ 6. Document ID: US 20020049894 A1

L9: Entry 6 of 34

File: PGPB

Apr 25, 2002

PGPUB-DOCUMENT-NUMBER: 20020049894  
PGPUB-FILING-TYPE: new  
DOCUMENT-IDENTIFIER: US 20020049894 A1

TITLE: Method and apparatus for interfacing a processor to a coprocessor

PUBLICATION-DATE: April 25, 2002

## INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Moyer, William C.	Dripping Springs	TX	US	
Arends, John	Austin	TX	US	
Scott, Jeffrey W.	Austin	TX	US	

US-CL-CURRENT: 712/34

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KMC
Draw Desc	Image									

☐ 7. Document ID: US 6606743 B1

L9: Entry 7 of 34

File: USPT

Aug 12, 2003

US-PAT-NO: 6606743  
DOCUMENT-IDENTIFIER: US 6606743 B1

TITLE: Real time program language accelerator

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KMC
Draw Desc	Image									

☐ 8. Document ID: US 6571328 B2

L9: Entry 8 of 34

File: USPT

May 27, 2003

US-PAT-NO: 6571328  
DOCUMENT-IDENTIFIER: US 6571328 B2

TITLE: Method and apparatus for obtaining a scalar value directly from a vector

register

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw Desc	Image									

☐ 9. Document ID: US 6505290 B1

L9: Entry 9 of 34

File: USPT

Jan 7, 2003

US-PAT-NO: 6505290

DOCUMENT-IDENTIFIER: US 6505290 B1

TITLE: Method and apparatus for interfacing a processor to a coprocessor

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw Desc	Image									

☐ 10. Document ID: US 6470380 B1

L9: Entry 10 of 34

File: USPT

Oct 22, 2002

US-PAT-NO: 6470380

DOCUMENT-IDENTIFIER: US 6470380 B1

**\*\* See image for Certificate of Correction \*\***

TITLE: Signal processing device accessible as memory

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw Desc	Image									

☐ 11. Document ID: US 6434688 B1

L9: Entry 11 of 34

File: USPT

Aug 13, 2002

US-PAT-NO: 6434688

DOCUMENT-IDENTIFIER: US 6434688 B1

TITLE: Method and apparatus for providing and maximizing concurrent operations in a shared memory system which includes display memory

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw Desc	Image									

☐ 12. Document ID: US 6430593 B1

L9: Entry 12 of 34

File: USPT

Aug 6, 2002

US-PAT-NO: 6430593

DOCUMENT-IDENTIFIER: US 6430593 B1

TITLE: Method, device and article of manufacture for efficient task scheduling in a multi-tasking preemptive priority-based real-time operating system

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMC

☐ 13. Document ID: US 6414687 B1

L9: Entry 13 of 34

File: USPT

Jul 2, 2002

US-PAT-NO: 6414687

DOCUMENT-IDENTIFIER: US 6414687 B1

**\*\* See image for Certificate of Correction \*\***

TITLE: Register setting-micro programming system

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMC

☐ 14. Document ID: US 6393545 B1

L9: Entry 14 of 34

File: USPT

May 21, 2002

US-PAT-NO: 6393545

DOCUMENT-IDENTIFIER: US 6393545 B1

**\*\* See image for Certificate of Correction \*\***

TITLE: Method apparatus and system for managing virtual memory with virtual-physical mapping

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMC

☐ 15. Document ID: US 6351789 B1

L9: Entry 15 of 34

File: USPT

Feb 26, 2002

US-PAT-NO: 6351789

DOCUMENT-IDENTIFIER: US 6351789 B1

TITLE: Built-in self-test circuit and method for validating an associative data array

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMC

☐ 16. Document ID: US 6336180 B1

L9: Entry 16 of 34

File: USPT

Jan 1, 2002

US-PAT-NO: 6336180

DOCUMENT-IDENTIFIER: US 6336180 B1

**\*\* See image for Certificate of Correction \*\***

TITLE: Method, apparatus and system for managing virtual memory with virtual-physical mapping

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMIC

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☐ 17. Document ID: US 6332215 B1

L9: Entry 17 of 34

File: USPT

Dec 18, 2001

US-PAT-NO: 6332215

DOCUMENT-IDENTIFIER: US 6332215 B1

**\*\* See image for Certificate of Correction \*\***

TITLE: Java virtual machine hardware for RISC and CISC processors

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMIC

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☐ 18. Document ID: US 6330659 B1

L9: Entry 18 of 34

File: USPT

Dec 11, 2001

US-PAT-NO: 6330659

DOCUMENT-IDENTIFIER: US 6330659 B1

TITLE: Hardware accelerator for an object-oriented programming language

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMIC

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☐ 19. Document ID: US 6327647 B1

L9: Entry 19 of 34

File: USPT

Dec 4, 2001

US-PAT-NO: 6327647

DOCUMENT-IDENTIFIER: US 6327647 B1

TITLE: Method and apparatus for interfacing a processor to a coprocessor

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMIC

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☐ 20. Document ID: US 6311258 B1

L9: Entry 20 of 34

File: USPT

Oct 30, 2001

US-PAT-NO: 6311258

DOCUMENT-IDENTIFIER: US 6311258 B1

**\*\* See image for Certificate of Correction \*\***

TITLE: Data buffer apparatus and method for storing graphical data using data

encoders and decoders

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw Desc	Image									

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Term	Documents
(8 AND 1).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	34
(L1 AND L8).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	34

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Search Results - Record(s) 1 through 15 of 15 returned.

☐ 1. Document ID: US 20030018917 A1

L7: Entry 1 of 15

File: PGPB

Jan 23, 2003

PGPUB-DOCUMENT-NUMBER: 20030018917

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20030018917 A1

TITLE: Method and apparatus for delivering digital media using packetized encryption data

PUBLICATION-DATE: January 23, 2003

## INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Brown, Matthew W. SR.	Charlotte	NC	US	

US-CL-CURRENT: 713/201

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC
Draw Desc	Image										

☐ 2. Document ID: US 20020151992 A1

L7: Entry 2 of 15

File: PGPB

Oct 17, 2002

PGPUB-DOCUMENT-NUMBER: 20020151992

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020151992 A1

TITLE: Media recording device with packet data interface

PUBLICATION-DATE: October 17, 2002

## INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Hoffberg, Steven M.	West Harrison	NY	US	
Hoffberg-Borghesani, Linda I.	Acton	MA	US	

US-CL-CURRENT: 700/83; 700/17, 700/18, 700/86, 700/87

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC
Draw Desc	Image										

☐ 3. Document ID: US 20020099756 A1

L7: Entry 3 of 15

File: PGPB

Jul 25, 2002



PGPUB-DOCUMENT-NUMBER: 20020099756  
PGPUB-FILING-TYPE: new  
DOCUMENT-IDENTIFIER: US 20020099756 A1

TITLE: Task concurrency management design method

PUBLICATION-DATE: July 25, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Catthoor, Francky	Temse		BE	
Yang, Peng	Leuven		BE	
Wong, Chun	Leuven		BE	
Marchal, Paul	Blanden		BE	
Prayati, Aggeliki	Athens		GR	
Cossement, Nathalie	Rekkem		BE	
Lauwereins, Rudy	Winksele		BE	

US-CL-CURRENT: 709/102

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw Desc	Image									

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☐ 4. Document ID: US 20020087829 A1

L7: Entry 4 of 15

File: PGPB

Jul 4, 2002

PGPUB-DOCUMENT-NUMBER: 20020087829  
PGPUB-FILING-TYPE: new  
DOCUMENT-IDENTIFIER: US 20020087829 A1

TITLE: Re-targetable communication system

PUBLICATION-DATE: July 4, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Snyder, Walter L.	San Jose	CA	US	
Tsui, Ernest T.	Cupertino	CA	US	

US-CL-CURRENT: 712/34

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw Desc	Image									

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☐ 5. Document ID: US 20020059426 A1

L7: Entry 5 of 15

File: PGPB

May 16, 2002

PGPUB-DOCUMENT-NUMBER: 20020059426  
PGPUB-FILING-TYPE: new  
DOCUMENT-IDENTIFIER: US 20020059426 A1

TITLE: Technique for assigning schedule resources to multiple ports in correct proportions

PUBLICATION-DATE: May 16, 2002

## INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Brinkerhoff, Kenneth W.	Mission Viejo	CA	US	
Boese, Wayne P.	Costa Mesa	CA	US	
Hutchins, Robert C.	Mission Viejo	CA	US	
Wong, Stanley	Santa Ana	CA	US	

US-CL-CURRENT: 709/226; 709/238

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

K00C

☐ 6. Document ID: US 20020034162 A1

L7: Entry 6 of 15

File: PGPB

Mar 21, 2002

PGPUB-DOCUMENT-NUMBER: 20020034162

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020034162 A1

TITLE: Technique for implementing fractional interval times for fine granularity bandwidth allocation

PUBLICATION-DATE: March 21, 2002

## INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Brinkerhoff, Kenneth W.	Mission Viejo	CA	US	
Boese, Wayne P.	Costa Mesa	CA	US	
Hutchins, Robert C.	Mission Viejo	CA	US	
Wong, Stanley	Santa Ana	CA	US	

US-CL-CURRENT: 370/229; 370/230, 370/235

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

K00C

☐ 7. Document ID: US 20010055130 A1

L7: Entry 7 of 15

File: PGPB

Dec 27, 2001

PGPUB-DOCUMENT-NUMBER: 20010055130

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20010055130 A1

TITLE: Apparatus, product, and method of trapping using a distance buffer

PUBLICATION-DATE: December 27, 2001

## INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Geurts, Wim	Gent		BE	
Van Bael, Kristiaan K.A.	Hasselt		BE	
Fransen, Wim J.C.	Bornem		BE	

US-CL-CURRENT: 358/530; 345/619

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWOC
Draw Desc	Image									

☐ 8. Document ID: US 6415369 B1

L7: Entry 8 of 15

File: USPT

Jul 2, 2002

US-PAT-NO: 6415369

DOCUMENT-IDENTIFIER: US 6415369 B1

TITLE: Shared devices and memory using split bus and time slot interface bus arbitration

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWOC
Draw Desc	Image									

☐ 9. Document ID: US 6400996 B1

L7: Entry 9 of 15

File: USPT

Jun 4, 2002

US-PAT-NO: 6400996

DOCUMENT-IDENTIFIER: US 6400996 B1

TITLE: Adaptive pattern recognition based control system and method

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWOC
Draw Desc	Image									

☐ 10. Document ID: US 6298370 B1

L7: Entry 10 of 15

File: USPT

Oct 2, 2001

US-PAT-NO: 6298370

DOCUMENT-IDENTIFIER: US 6298370 B1

TITLE: Computer operating process allocating tasks between first and second processors at run time based upon current processor load

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWOC
Draw Desc	Image									

☐ 11. Document ID: US 6279144 B1

L7: Entry 11 of 15

File: USPT

Aug 21, 2001

US-PAT-NO: 6279144

DOCUMENT-IDENTIFIER: US 6279144 B1

TITLE: Provably correct storage arrays

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw	Desc	Image							

KMIC

☐ 12. Document ID: US 6179489 B1

L7: Entry 12 of 15

File: USPT

Jan 30, 2001

US-PAT-NO: 6179489

DOCUMENT-IDENTIFIER: US 6179489 B1

TITLE: Devices, methods, systems and software products for coordination of computer main microprocessor and second microprocessor coupled thereto

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw	Desc	Image							

KMIC

☐ 13. Document ID: US 6105119 A

L7: Entry 13 of 15

File: USPT

Aug 15, 2000

US-PAT-NO: 6105119

DOCUMENT-IDENTIFIER: US 6105119 A

TITLE: Data transfer circuitry, DSP wrapper circuitry and improved processor devices, methods and systems

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw	Desc	Image							

KMIC

☐ 14. Document ID: US 5995425 A

L7: Entry 14 of 15

File: USPT

Nov 30, 1999

US-PAT-NO: 5995425

DOCUMENT-IDENTIFIER: US 5995425 A

TITLE: Design of provably correct storage arrays

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw	Desc	Image							

KMIC

☐ 15. Document ID: US 5909559 A

L7: Entry 15 of 15

File: USPT

Jun 1, 1999

US-PAT-NO: 5909559

DOCUMENT-IDENTIFIER: US 5909559 A

TITLE: Bus bridge device including data bus of first width for a first processor, memory controller, arbiter circuit and second processor having a different second data width

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
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KWC

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Term	Documents
DSL.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	4255
DSL.S.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	112
ADSL.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	3363
ADSL.S.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	32
DIGITAL.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	844938
DIGITAL.S.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	224
SUBSCRIBER.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	91437
SUBSCRIBERS.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	33300
(6 AND ((DSL OR ADSL) OR (SUBSCRIBER NEAR1 DIGITAL))).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	15
(L6 AND (DSL OR ADSL OR DIGITAL NEAR1 SUBSCRIBER)).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	15

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Search Results - Record(s) 1 through 6 of 6 returned.

☐ 1. Document ID: US 20020099756 A1

L12: Entry 1 of 6

File: PGPB

Jul 25, 2002

PGPUB-DOCUMENT-NUMBER: 20020099756

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020099756 A1

TITLE: Task concurrency management design method

PUBLICATION-DATE: July 25, 2002

## INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Catthoor, Francky	Temse		BE	
Yang, Peng	Leuven		BE	
Wong, Chun	Leuven		BE	
Marchal, Paul	Blanden		BE	
Prayati, Aggeliki	Athens		GR	
Cossement, Nathalie	Rekkem		BE	
Lauwereins, Rudy	Winksele		BE	

US-CL-CURRENT: 709/102

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
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[KWC](#)☐ 2. Document ID: US 6415369 B1

L12: Entry 2 of 6

File: USPT

Jul 2, 2002

US-PAT-NO: 6415369

DOCUMENT-IDENTIFIER: US 6415369 B1

TITLE: Shared devices and memory using split bus and time slot interface bus arbitration

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
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[KWC](#)☐ 3. Document ID: US 6298370 B1

L12: Entry 3 of 6

File: USPT

Oct 2, 2001

US-PAT-NO: 6298370

DOCUMENT-IDENTIFIER: US 6298370 B1

TITLE: Computer operating process allocating tasks between first and second processors at run time based upon current processor load

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw Desc	Image									

☐ 4. Document ID: US 6179489 B1

L12: Entry 4 of 6

File: USPT

Jan 30, 2001

US-PAT-NO: 6179489

DOCUMENT-IDENTIFIER: US 6179489 B1

TITLE: Devices, methods, systems and software products for coordination of computer main microprocessor and second microprocessor coupled thereto

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw Desc	Image									

☐ 5. Document ID: US 6105119 A

L12: Entry 5 of 6

File: USPT

Aug 15, 2000

US-PAT-NO: 6105119

DOCUMENT-IDENTIFIER: US 6105119 A

TITLE: Data transfer circuitry, DSP wrapper circuitry and improved processor devices, methods and systems

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw Desc	Image									

☐ 6. Document ID: US 5909559 A

L12: Entry 6 of 6

File: USPT

Jun 1, 1999

US-PAT-NO: 5909559

DOCUMENT-IDENTIFIER: US 5909559 A

TITLE: Bus bridge device including data bus of first width for a first processor, memory controller, arbiter circuit and second processor having a different second data width

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw Desc	Image									

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Term	Documents
HARDWARE.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	255594
HARDWARES.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1590
ACCELERATOR\$	0
ACCELERATOR.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	101482
ACCELERATORA.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
ACCELERATORADDITIVE.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
ACCELERATORAPPLICATIONS.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
ACCELERATORAS.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
ACCELERATORCATALYST.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
ACCELERATORCC*.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
ACCELERATORCHANGE.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
(L11 AND HARDWARE NEAR3 ACCELERATOR\$).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	6

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Term	Documents
HARDWARE.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	255594
HARDWARES.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1590
ACCELERATOR\$	0
ACCELERATOR.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	101482
ACCELERATORA.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
ACCELERATORADDITIVE.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
ACCELERATORAPPLICATIONS.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
ACCELERATORAS.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
ACCELERATORCATALYST.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
ACCELERATORCC*.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
ACCELERATORCHANGE.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
(L11 AND HARDWARE NEAR3 ACCELERATOR\$).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	6

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## Search History

DATE: Tuesday, January 28, 2003   [Printable Copy](#)   [Create Case](#)

Set Name Query  
side by side

Hit Count Set Name  
result set

*DB=USPT,PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=OR*

<u>L12</u>	L11 and hardware near3 accelerator\$	6	<u>L12</u>
<u>L11</u>	l1 and digital near1 subscriber	2330	<u>L11</u>
<u>L10</u>	asymetric and l7	0	<u>L10</u>
<u>L9</u>	asymetric and l8	0	<u>L9</u>
<u>L8</u>	L7 and ram	7	<u>L8</u>
<u>L7</u>	L6 and (dsl or adsl or digital near1 subscriber)	15	<u>L7</u>
<u>L6</u>	hardware near3 accelerator\$	805	<u>L6</u>
<u>L5</u>	L1 and hardware near3 accelerator\$	8	<u>L5</u>
<u>L4</u>	L1 and hardware near3 accelerator\$ near8 (sav\$3 or stor\$3 or kept) near5 (condition\$ or parameter\$ or value\$)	0	<u>L4</u>
<u>L3</u>	L1 hardware near3 accelerator\$ near8 (sav\$3 or stor\$3 or kept) near5 (condition\$ or parameter\$ or value\$)	3370	<u>L3</u>
<u>L2</u>	L1 hardware near3 accelerator\$	4160	<u>L2</u>
<u>L1</u>	ADSL	3363	<u>L1</u>

END OF SEARCH HISTORY

**WEST**[Generate Collection](#)[Print](#)

Search Results - Record(s) 1 through 7 of 7 returned.

☐ 1. Document ID: US 20030018917 A1

L4: Entry 1 of 7

File: PGPB

Jan 23, 2003

PGPUB-DOCUMENT-NUMBER: 20030018917  
PGPUB-FILING-TYPE: new  
DOCUMENT-IDENTIFIER: US 20030018917 A1

TITLE: Method and apparatus for delivering digital media using packetized encryption data

PUBLICATION-DATE: January 23, 2003

## INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Brown, Matthew W. SR.	Charlotte	NC	US	

US-CL-CURRENT: 713/201

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw	Desc	Image								

☐ 2. Document ID: US 20020087829 A1

L4: Entry 2 of 7

File: PGPB

Jul 4, 2002

PGPUB-DOCUMENT-NUMBER: 20020087829  
PGPUB-FILING-TYPE: new  
DOCUMENT-IDENTIFIER: US 20020087829 A1

TITLE: Re-targetable communication system

PUBLICATION-DATE: July 4, 2002

## INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Snyder, Walter L.	San Jose	CA	US	
Tsui, Ernest T.	Cupertino	CA	US	

US-CL-CURRENT: 712/34

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw	Desc	Image								

☐ 3. Document ID: US 20020059426 A1

L4: Entry 3 of 7

File: PGPB

May 16, 2002

PGPUB-DOCUMENT-NUMBER: 20020059426  
PGPUB-FILING-TYPE: new  
DOCUMENT-IDENTIFIER: US 20020059426 A1

TITLE: Technique for assigning schedule resources to multiple ports in correct proportions

PUBLICATION-DATE: May 16, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Brinkerhoff, Kenneth W.	Mission Viejo	CA	US	
Boese, Wayne P.	Costa Mesa	CA	US	
Hutchins, Robert C.	Mission Viejo	CA	US	
Wong, Stanley	Santa Ana	CA	US	

US-CL-CURRENT: 709/226; 709/238

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw	Desc	Image								

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☐ 4. Document ID: US 20020034162 A1

L4: Entry 4 of 7

File: PGPB

Mar 21, 2002

PGPUB-DOCUMENT-NUMBER: 20020034162  
PGPUB-FILING-TYPE: new  
DOCUMENT-IDENTIFIER: US 20020034162 A1

TITLE: Technique for implementing fractional interval times for fine granularity bandwidth allocation

PUBLICATION-DATE: March 21, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Brinkerhoff, Kenneth W.	Mission Viejo	CA	US	
Boese, Wayne P.	Costa Mesa	CA	US	
Hutchins, Robert C.	Mission Viejo	CA	US	
Wong, Stanley	Santa Ana	CA	US	

US-CL-CURRENT: 370/229; 370/230, 370/235

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw	Desc	Image								

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☒ 5. Document ID: US 20010055130 A1

L4: Entry 5 of 7

File: PGPB

Dec 27, 2001

PGPUB-DOCUMENT-NUMBER: 20010055130  
PGPUB-FILING-TYPE: new  
DOCUMENT-IDENTIFIER: US 20010055130 A1

TITLE: Apparatus, product, and method of trapping using a distance buffer

PUBLICATION-DATE: December 27, 2001

## INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Geurts, Wim	Gent		BE	
Van Bael, Kristiaan K.A.	Hasselt		BE	
Fransen, Wim J.C.	Bornem		BE	

US-CL-CURRENT: 358/530; 345/619

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMC

☐ 6. Document ID: US 6279144 B1

L4: Entry 6 of 7

File: USPT

Aug 21, 2001

US-PAT-NO: 6279144

DOCUMENT-IDENTIFIER: US 6279144 B1

TITLE: Provably correct storage arrays

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMC

☐ 7. Document ID: US 5995425 A

L4: Entry 7 of 7

File: USPT

Nov 30, 1999

US-PAT-NO: 5995425

DOCUMENT-IDENTIFIER: US 5995425 A

TITLE: Design of provably correct storage arrays

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMC

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Term	Documents
(3 NOT 1).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	7
(L3 NOT L1).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	7

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Term	Documents
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(L3 NOT L1).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	7

Database:

US Patents Full-Text Database  
 US Pre-Grant Publication Full-Text Database  
 JPO Abstracts Database  
 EPO Abstracts Database  
 Derwent World Patents Index  
 IBM Technical Disclosure Bulletins

Search:

L4

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## Search History

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 side by side

Hit Count   Set Name  
 result set

*DB=USPT,PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=OR*

<u>L4</u>	L3 not l1	7	<u>L4</u>
<u>L3</u>	(dsl or digital near1 subscriber) and hardware near3 accelerator\$	13	<u>L3</u>
<u>L2</u>	dsl and hardware near3 accelerator\$	10	<u>L2</u>
<u>L1</u>	ADSL and hardware near3 accelerator\$	8	<u>L1</u>

END OF SEARCH HISTORY

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Search Results - Record(s) 1 through 15 of 15 returned.

☐ 1. Document ID: US 20020172356 A1

L7: Entry 1 of 15

File: PGPB

Nov 21, 2002

PGPUB-DOCUMENT-NUMBER: 20020172356  
PGPUB-FILING-TYPE: new  
DOCUMENT-IDENTIFIER: US 20020172356 A1

TITLE: Information security device, exponentiation device, modular exponentiation device, and elliptic curve exponentiation device

PUBLICATION-DATE: November 21, 2002

## INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Ono, Takatoshi	Aichi-ken		JP	
Matsuzaki, Natsume	Mino-shi		JP	
Nakano, Toshihisa	Neyagawa-shi		JP	

US-CL-CURRENT: 380/28; 380/30

<a href="#">Full</a>	<a href="#">Title</a>	<a href="#">Citation</a>	<a href="#">Front</a>	<a href="#">Review</a>	<a href="#">Classification</a>	<a href="#">Date</a>	<a href="#">Reference</a>	<a href="#">Sequences</a>	<a href="#">Attachments</a>
<a href="#">Draw</a>	<a href="#">Desc</a>	<a href="#">Image</a>							

[K00C](#)☐ 2. Document ID: US 6373493 B1

L7: Entry 2 of 15

File: USPT

Apr 16, 2002

US-PAT-NO: 6373493  
DOCUMENT-IDENTIFIER: US 6373493 B1

TITLE: Hardware graphics accelerator having access to multiple types of memory including cached memory

<a href="#">Full</a>	<a href="#">Title</a>	<a href="#">Citation</a>	<a href="#">Front</a>	<a href="#">Review</a>	<a href="#">Classification</a>	<a href="#">Date</a>	<a href="#">Reference</a>	<a href="#">Sequences</a>	<a href="#">Attachments</a>
<a href="#">Draw</a>	<a href="#">Desc</a>	<a href="#">Image</a>							

[K00C](#)☐ 3. Document ID: US 6356636 B1

L7: Entry 3 of 15

File: USPT

Mar 12, 2002

US-PAT-NO: 6356636  
DOCUMENT-IDENTIFIER: US 6356636 B1

TITLE: Circuit and method for fast modular multiplication

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KVMC

☐ 4. Document ID: US 6275068 B1

L7: Entry 4 of 15

File: USPT

Aug 14, 2001

US-PAT-NO: 6275068

DOCUMENT-IDENTIFIER: US 6275068 B1

TITLE: Programmable clock delay

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KVMC

☐ 5. Document ID: US 6182104 B1

L7: Entry 5 of 15

File: USPT

Jan 30, 2001

US-PAT-NO: 6182104

DOCUMENT-IDENTIFIER: US 6182104 B1

TITLE: Circuit and method of modulo multiplication

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KVMC

☐ 6. Document ID: US 5949439 A

L7: Entry 6 of 15

File: USPT

Sep 7, 1999

US-PAT-NO: 5949439

DOCUMENT-IDENTIFIER: US 5949439 A

TITLE: Computing apparatus and operating method using software queues to improve graphics performance

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KVMC

☐ 7. Document ID: US 5845327 A

L7: Entry 7 of 15

File: USPT

Dec 1, 1998

US-PAT-NO: 5845327

DOCUMENT-IDENTIFIER: US 5845327 A

TITLE: Cache coherency where multiple processors may access the same data over independent access paths

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KVMC



Sep 1, 1998

DOCUMENT-IDENTIFIER: US 5801711 A

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Drawn Desc	Image								

Kyöte

Jul 21, 1998

DOCUMENT-IDENTIFIER: US 5784075 A

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draws Desc	Image								



May 19, 1998

DOCUMENT-IDENTIFIER: US 5754556 A

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KUBIC

Dec 9, 1997

DOCUMENT-IDENTIFIER: US 5696944 A

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw	Desc	Image							

KUBIC

☐ 12. Document ID: US 5489902 A

L7: Entry 12 of 15

File: USPT

Feb 6, 1996

US-PAT-NO: 5489902

DOCUMENT-IDENTIFIER: US 5489902 A

TITLE: Dynamic power saving video DAC

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw Desc	Image									

☐ 13. Document ID: US 4839851 A

L7: Entry 13 of 15

File: USPT

Jun 13, 1989

US-PAT-NO: 4839851

DOCUMENT-IDENTIFIER: US 4839851 A

TITLE: Programmable data path device

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw Desc	Image									

☐ 14. Document ID: EP 1241892 A1

L7: Entry 14 of 15

File: DWPI

Sep 18, 2002

DERWENT-ACC-NO: 2003-031802

DERWENT-WEEK: 200303

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TITLE: Hardware-accelerator for use in a video processing system carries out more image processing steps than existing accelerators

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw Desc	Image									

☐ 15. Document ID: EP 992895 A1 JP 2000215057 A

L7: Entry 15 of 15

File: DWPI

Apr 12, 2000

DERWENT-ACC-NO: 2000-273376

DERWENT-WEEK: 200042

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TITLE: Data processing apparatus using hardware acceleration has hardware accelerator coupled to random access memory and processor coupling hardware accelerator to random access memory

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw Desc	Clip Img	Image								

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Term	Documents
HARDWARE.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	255594
HARDWARES.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1590
RAM.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	282425
RAMS.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	35667
RANDOM.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	372859
RANDOMS.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	51
ACCESS.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	793067
ACCESSES.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	80445
ACCELERATOR\$	0
ACCELERATOR.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	101482
(HARDWARE NEAR3 ACCELERATOR\$ NEAR10 (RAM OR RANDOM NEAR1 ACCESS)).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	15

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Search Results - Record(s) 1 through 15 of 15 returned.

☐ 1. Document ID: US 20020172356 A1

L7: Entry 1 of 15

File: PGPB

Nov 21, 2002

PGPUB-DOCUMENT-NUMBER: 20020172356  
PGPUB-FILING-TYPE: new  
DOCUMENT-IDENTIFIER: US 20020172356 A1

TITLE: Information security device, exponentiation device, modular exponentiation device, and elliptic curve exponentiation device

PUBLICATION-DATE: November 21, 2002

## INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Ono, Takatoshi	Aichi-ken		JP	
Matsuzaki, Natsume	Mino-shi		JP	
Nakano, Toshihisa	Neyagawa-shi		JP	

US-CL-CURRENT: 380/28; 380/30

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Drawn Desc	Image									

☐ 2. Document ID: US 6373493 B1

L7: Entry 2 of 15

File: USPT

Apr 16, 2002

US-PAT-NO: 6373493  
DOCUMENT-IDENTIFIER: US 6373493 B1

TITLE: Hardware graphics accelerator having access to multiple types of memory including cached memory

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Drawn Desc	Image									

☐ 3. Document ID: US 6356636 B1

L7: Entry 3 of 15

File: USPT

Mar 12, 2002

US-PAT-NO: 6356636  
DOCUMENT-IDENTIFIER: US 6356636 B1

TITLE: Circuit and method for fast modular multiplication

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMC

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☐ 4. Document ID: US 6275068 B1

L7: Entry 4 of 15

File: USPT

Aug 14, 2001

US-PAT-NO: 6275068

DOCUMENT-IDENTIFIER: US 6275068 B1

TITLE: Programmable clock delay

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMC

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☐ 5. Document ID: US 6182104 B1

L7: Entry 5 of 15

File: USPT

Jan 30, 2001

US-PAT-NO: 6182104

DOCUMENT-IDENTIFIER: US 6182104 B1

TITLE: Circuit and method of modulo multiplication

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMC

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☐ 6. Document ID: US 5949439 A

L7: Entry 6 of 15

File: USPT

Sep 7, 1999

US-PAT-NO: 5949439

DOCUMENT-IDENTIFIER: US 5949439 A

TITLE: Computing apparatus and operating method using software queues to improve graphics performance

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMC

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☐ 7. Document ID: US 5845327 A

L7: Entry 7 of 15

File: USPT

Dec 1, 1998

US-PAT-NO: 5845327

DOCUMENT-IDENTIFIER: US 5845327 A

TITLE: Cache coherency where multiple processors may access the same data over independent access paths

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMC

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☐ 8. Document ID: US 5801711 A

L7: Entry 8 of 15

File: USPT

Sep 1, 1998

US-PAT-NO: 5801711

DOCUMENT-IDENTIFIER: US 5801711 A

TITLE: Polyline and triangle strip data management techniques for enhancing performance of computer graphics system

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KVMC

---

☐ 9. Document ID: US 5784075 A

L7: Entry 9 of 15

File: USPT

Jul 21, 1998

US-PAT-NO: 5784075

DOCUMENT-IDENTIFIER: US 5784075 A

TITLE: Memory mapping techniques for enhancing performance of computer graphics system

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KVMC

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☒ 10. Document ID: US 5754556 A

L7: Entry 10 of 15

File: USPT

May 19, 1998

US-PAT-NO: 5754556

DOCUMENT-IDENTIFIER: US 5754556 A

TITLE: Semiconductor memory tester with hardware accelerators

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KVMC

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☐ 11. Document ID: US 5696944 A

L7: Entry 11 of 15

File: USPT

Dec 9, 1997

US-PAT-NO: 5696944

DOCUMENT-IDENTIFIER: US 5696944 A

TITLE: Computer graphics system having double buffered vertex ram with granularity

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KVMC

☐ 12. Document ID: US 5489902 A

L7: Entry 12 of 15

File: USPT

Feb 6, 1996

US-PAT-NO: 5489902

DOCUMENT-IDENTIFIER: US 5489902 A

TITLE: Dynamic power saving video DAC

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KVMC
Draw Desc	Image									

☐ 13. Document ID: US 4839851 A

L7: Entry 13 of 15

File: USPT

Jun 13, 1989

US-PAT-NO: 4839851

DOCUMENT-IDENTIFIER: US 4839851 A

TITLE: Programmable data path device

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KVMC
Draw Desc	Image									

☐ 14. Document ID: EP 1241892 A1

L7: Entry 14 of 15

File: DWPI

Sep 18, 2002

DERWENT-ACC-NO: 2003-031802

DERWENT-WEEK: 200303

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TITLE: Hardware-accelerator for use in a video processing system carries out more image processing steps than existing accelerators

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KVMC
Draw Desc	Image									

☐ 15. Document ID: EP 992895 A1 JP 2000215057 A

L7: Entry 15 of 15

File: DWPI

Apr 12, 2000

DERWENT-ACC-NO: 2000-273376

DERWENT-WEEK: 200042

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TITLE: Data processing apparatus using hardware acceleration has hardware accelerator coupled to random access memory and processor coupling hardware accelerator to random access memory

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KVMC
Draw Desc	Clip Img	Image								

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Term	Documents
HARDWARE.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	255594
HARDWARES.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1590
RAM.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	282425
RAMS.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	35667
RANDOM.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	372859
RANDOMS.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	51
ACCESS.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	793067
ACCESSES.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	80445
ACCELERATOR\$	0
ACCELERATOR.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	101482
(HARDWARE NEAR3 ACCELERATOR\$ NEAR10 (RAM OR RANDOM NEAR1 ACCESS)).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	15

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Search Results - Record(s) 61 through 69 of 69 returned.

☐ 61. Document ID: US 6052380 A

L19: Entry 61 of 69

File: USPT

Apr 18, 2000

US-PAT-NO: 6052380

DOCUMENT-IDENTIFIER: US 6052380 A

TITLE: Network adapter utilizing an ethernet protocol and utilizing a digital subscriber line physical layer driver for improved performance

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KMOC
Draw Desc	Image									

☐ 62. Document ID: US 6049531 A

L19: Entry 62 of 69

File: USPT

Apr 11, 2000

US-PAT-NO: 6049531

DOCUMENT-IDENTIFIER: US 6049531 A

TITLE: Real-time multimedia conferencing over an ATM network using an intelligent ATM ADSL modem and ADSL access

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KMOC
Draw Desc	Image									

☐ 63. Document ID: US 6044145 A

L19: Entry 63 of 69

File: USPT

Mar 28, 2000

US-PAT-NO: 6044145

DOCUMENT-IDENTIFIER: US 6044145 A

TITLE: Telecommutable platform

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KMOC
Draw Desc	Image									

☐ 64. Document ID: US 6014412 A

L19: Entry 64 of 69

File: USPT

Jan 11, 2000

US-PAT-NO: 6014412

DOCUMENT-IDENTIFIER: US 6014412 A

TITLE: Digital radio frequency interference canceller

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KWIC

☐ 65. Document ID: US 5909463 A

L19: Entry 65 of 69

File: USPT

Jun 1, 1999

US-PAT-NO: 5909463

DOCUMENT-IDENTIFIER: US 5909463 A

TITLE: Single-chip software configurable transceiver for asymmetric communication system

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KWIC

☐ 66. Document ID: US 5905781 A

L19: Entry 66 of 69

File: USPT

May 18, 1999

US-PAT-NO: 5905781

DOCUMENT-IDENTIFIER: US 5905781 A

TITLE: Communication server apparatus and method

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KWIC

☐ 67. Document ID: US 5889856 A

L19: Entry 67 of 69

File: USPT

Mar 30, 1999

US-PAT-NO: 5889856

DOCUMENT-IDENTIFIER: US 5889856 A

TITLE: ADSL integrated line card with digital splitter and POTS CODEC without bulky analog splitter

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KWIC

☒ 68. Document ID: US 5883907 A

L19: Entry 68 of 69

File: USPT

Mar 16, 1999

US-PAT-NO: 5883907

DOCUMENT-IDENTIFIER: US 5883907 A

TITLE: Asymmetrical digital subscriber line (ADSL) block encoder circuit and method of operation

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KWC

☐ 69. Document ID: US 5596604 A

L19: Entry 69 of 69

File: USPT

Jan 21, 1997

US-PAT-NO: 5596604

DOCUMENT-IDENTIFIER: US 5596604 A

TITLE: Multicarrier modulation transmission system with variable delay

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KWC

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Term	Documents
(16 NOT 17).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	69
(L16 NOT L17).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	69

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Term	Documents
(16 NOT 17).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	69
(L16 NOT L17).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	69

Database:

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L19

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## Search History

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<u>Set Name</u> side by side	<u>Query</u>	<u>Hit Count</u>	<u>Set Name</u> result set
	<i>DB=USPT,PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>		
<u>L19</u>	l16 not l17	69	<u>L19</u>
<u>L18</u>	l16 not l15	0	<u>L18</u>
<u>L17</u>	digital near1 signal and (adsl\$ or asymmetric near1 digital near1 subscriber or asymmetric near1 dsl\$) near4 (plur\$6 or multiple or multi\$5 or two) and (ram or random near1 access) near9 (16 or sixteen)	15	<u>L17</u>
<u>L16</u>	digital near1 signal and (adsl\$ or asymmetric near1 digital near1 subscriber or asymmetric near1 dsl\$) near4 (plur\$6 or multiple or multi\$5 or two) and (ram or random near1 access)	84	<u>L16</u>
<u>L15</u>	digital near1 signal and (adsl\$ or asymmetric near1 digital near1 subscriber or asymmetric near1 dsl\$) near6 (plur\$6 or multiple or multi\$5 or two) and (ram or random near1 access)	114	<u>L15</u>
<u>L14</u>	(adsl\$ or asymmetric near1 digital near1 subscriber or asymmetric near1 dsl\$) near6 (plur\$6 or multiple or multi\$5 or two) and (ram or random near1 access)	151	<u>L14</u>
<u>L13</u>	(adsl\$ or asymmetric near1 digital near1 subscriber or asymmetric near1 dsl\$) near4 (plur\$6 or multiple or multi\$5 or two) near8 (ram or random near1 access)	0	<u>L13</u>
<u>L12</u>	(adsl\$ or asymmetric near1 digital near1 subscriber or asymmetric near1 dsl\$) near4 (plur\$6 or multiple or multi\$5 or two)	456	<u>L12</u>
<u>L11</u>	(adsl\$ or asymmetric near1 digital near1 subscriber or asymmetric near1 dsl\$) near6 (plur\$6 or multiple or multi\$5 or two)	593	<u>L11</u>
<u>L10</u>	(adsl\$ or asymmetric near1 digital near1 subscriber or asymmetric dsl\$) near6 (plur\$6 or multiple or multi\$5 or two)	1195	<u>L10</u>
<u>L9</u>	(adsl or asymmetric) near6 (plur\$6 or multiple or multi\$5 or two)	707	<u>L9</u>
<u>L8</u>	digital near1 signal and l7	3	<u>L8</u>
<u>L7</u>	hardware near3 accelerator\$ near10 (ram or random near1 access)	15	<u>L7</u>
<u>L6</u>	hardware near3 accelerator\$ near10 (ram or random near1 access) near12 (16 or sixteen)	1	<u>L6</u>
<u>L5</u>	hardware near3 accelerator\$ near8 (ram or random near1 access) near10 (16 or sixteen)	1	<u>L5</u>
<u>L4</u>	L3 not l1	7	<u>L4</u>
<u>L3</u>	(dsl or digital near1 subscriber) and hardware near3 accelerator\$	13	<u>L3</u>
<u>L2</u>	dsl and hardware near3 accelerator\$	10	<u>L2</u>
<u>L1</u>	ADSL and hardware near3 accelerator\$	8	<u>L1</u>

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## Search Results -

Term	Documents
"4839851".DWPI,EPAB,JPAB,USPT,PGPB.	3
4839851S	0
ACCELERATOR\$	0
ACCELERATOR.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	4317
ACCELERATORAPPLICATIONS.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
ACCELERATORPEDALS.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
ACCELERATORS.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1033
ACCELERATORS/CURING.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	2
ACCELERATORS/DECELERATORS.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
ACCELERATORS/INHIBITORS.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
ACCELERATORS/PROMOTORS.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
(4839851.PN. AND ACCELERATOR\$).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	2

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<u>Set Name</u> side by side	<u>Query</u>	<u>Hit Count</u>	<u>Set Name</u> result set
	<i>DB=USPT,PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>		
<u>L20</u>	4839851.pn. and accelerator\$	2	<u>L20</u>
<u>L19</u>	116 not 117	69	<u>L19</u>
<u>L18</u>	116 not 115	0	<u>L18</u>
<u>L17</u>	digital near1 signal and (adsl\$ or asymmetric near1 digital near1 subscriber or asymmetric near1 dsl\$) near4 (plur\$6 or multiple or multi\$5 or two) and (ram or random near1 access) near9 (16 or sixteen)	15	<u>L17</u>
<u>L16</u>	digital near1 signal and (adsl\$ or asymmetric near1 digital near1 subscriber or asymmetric near1 dsl\$) near4 (plur\$6 or multiple or multi\$5 or two) and (ram or random near1 access)	84	<u>L16</u>
<u>L15</u>	digital near1 signal and (adsl\$ or asymmetric near1 digital near1 subscriber or asymmetric near1 dsl\$) near6 (plur\$6 or multiple or multi\$5 or two) and (ram or random near1 access)	114	<u>L15</u>
<u>L14</u>	(adsl\$ or asymmetric near1 digital near1 subscriber or asymmetric near1 dsl\$) near6 (plur\$6 or multiple or multi\$5 or two) and (ram or random near1 access)	151	<u>L14</u>
<u>L13</u>	(adsl\$ or asymmetric near1 digital near1 subscriber or asymmetric near1 dsl\$) near4 (plur\$6 or multiple or multi\$5 or two) near8 (ram or random near1 access)	0	<u>L13</u>
<u>L12</u>	(adsl\$ or asymmetric near1 digital near1 subscriber or asymmetric near1 dsl\$) near4 (plur\$6 or multiple or multi\$5 or two)	456	<u>L12</u>
<u>L11</u>	(adsl\$ or asymmetric near1 digital near1 subscriber or asymmetric near1 dsl\$) near6 (plur\$6 or multiple or multi\$5 or two)	593	<u>L11</u>
<u>L10</u>	(adsl\$ or asymmetric near1 digital near1 subscriber or asymmetric dsl\$) near6 (plur\$6 or multiple or multi\$5 or two)	1195	<u>L10</u>
<u>L9</u>	(adsl or asymmetric) near6 (plur\$6 or multiple or multi\$5 or two)	707	<u>L9</u>
<u>L8</u>	digital near1 signal and 17	3	<u>L8</u>
<u>L7</u>	hardware near3 accelerator\$ near10 (ram or random near1 access)	15	<u>L7</u>
<u>L6</u>	hardware near3 accelerator\$ near10 (ram or random near1 access) near12 (16 or sixteen)	1	<u>L6</u>
<u>L5</u>	hardware near3 accelerator\$ near8 (ram or random near1 access) near10 (16 or sixteen)	1	<u>L5</u>
<u>L4</u>	L3 not 11	7	<u>L4</u>
<u>L3</u>	(dsl or digital near1 subscriber) and hardware near3 accelerator\$	13	<u>L3</u>
<u>L2</u>	dsl and hardware near3 accelerator\$	10	<u>L2</u>
<u>L1</u>	ADSL and hardware near3 accelerator\$	8	<u>L1</u>

END OF SEARCH HISTORY